IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An analog DLL which buffers an external clock signal and uses the buffered clock signal as a reference clock signal, comprising:

a delay model for ~~modeling delay time for buffering the external clock signal~~ delaying a delayed clock signal;

a phase comparator for comparing ~~an~~ a phase of the reference clock signal with an phase of an outputted signal from the delay model;

a charge pump for pumping charges in response to an outputted signal from the phase comparator;

a loop filter for generating a reference voltage which is determined by a quantity of charges inputted from the charge pump;

a voltage control delay line which delays the reference clock signal for a predetermined time, and outputs the delayed clock signal to the delay model, where the predetermined time is determined by the reference voltage; and

a tracking ~~digital-analog~~ analog-digital converter which converts the reference voltage to a digital value, and stores the digital value for keeping the reference voltage safely, and outputs a tracking voltage which corresponds to the digital value to the loop filter,

wherein the tracking analog-digital converter includes:

a voltage comparator for comparing the reference voltage with the tracking voltage;

a counting means for counting in response to an outputted signal from the voltage comparator, and for outputting an counting signal;

a register for storing a digital value which corresponds to the counting signal; and

a digital-analog converting means for generating a voltage which corresponds to the digital value, and for outputting the voltage as the tracking voltage.

2. (Original) The analog DLL as recited in claim 1, wherein the tracking voltage is outputted to the loop filter during a standby mode.

3. (Original) The analog DLL as recited in claim 2, wherein the loop filter includes a capacitor for storing the reference voltage.

4. (Canceled)

5. (Currently Amended) The analog DLL as recited in claim 4 2, wherein the digital-analog converting means includes:

a main digital-analog converter which generates a first tracking voltage for a high speed tracking, where the first tracking voltage corresponds to predetermined upper bits of the digital value; and

a sub digital-analog converter which generates a second tracking voltage for correcting the first tracking voltage to be equal to the reference voltage, where the second tracking voltage corresponds to all the bits, except the predetermined upper bits, of the digital value.

6. (Original) The analog DLL as recited in claim 5, wherein the digital-analog converting means is provided with a binary-thermometer converter which converts the predetermined upper bits to a thermometer code, and outputs the converted thermometer code to the main digital-analog converter, where the main digital-analog converter is segment typed.

7. (Currently Amended) The analog DLL as recited in claim 4 2, a unit gain buffer is included for buffering an outputted signal from the main digital-analog converter and the sub digital-analog converter, and for outputting the buffered signal as the tracking voltage.

8. (Original) The analog DLL as recited in claim 7, a switch is included for transferring the tracking voltage outputted from the unit gain buffer to the loop filter.

9. (Original) The analog DLL as recited in claim 3, wherein the reference voltage is determined by charges pumped by the charge pump when the analog DLL is locked.

10. (Original) The analog DLL as recited in claim 7, wherein all the blocks except the register, the digital-analog converting means and the unit gain buffer become disabled during the standby mode.

11. (Currently Amended) An analog phase locked loop (PLL) which buffers an external clock signal and uses the buffered clock signal as a reference clock signal, comprising:

a delay model for ~~modeling delay time for buffering the external clock signal~~ delaying a modulated signal;

a phase comparator for comparing ~~an~~ a phase of the reference clock signal with an phase of an outputted signal from the delay model;

a charge pump for pumping charges in response to an outputted signal from the phase comparator;

a loop filter for generating a reference voltage which is determined by a quantity of charges inputted from the charge pump;

a voltage control oscillator which modulates a frequency of the reference clock signal, and outputs the modulated signal to the delay model; and

a tracking ~~digital-analog~~ analog-digital converter which converts the reference voltage to a digital value, and stores the digital value for keeping the reference voltage safely, and outputs a tracking voltage which corresponds to the digital value to the loop filter,

wherein the tracking analog-digital converter includes:

a voltage comparator for comparing the reference voltage with the tracking voltage;

a counting means for counting in response to an outputted signal from the voltage comparator, and for outputting an counting signal;

a register for storing a digital value which corresponds to the counting signal; and

a digital-analog converting means for generating a voltage which corresponds to the digital value, and for outputting the voltage as the tracking voltage.

12. (Original) The analog PLL as recited in claim 11, wherein the tracking voltage is outputted to the loop filter during a standby mode.

13. (Original) The analog PLL as recited in claim 12, wherein the loop filter includes a capacitor for storing the reference voltage.

14. (Canceled)

15. (Currently Amended) The analog DLL as recited in claim ~~14~~ 12, wherein the digital-analog converting means includes:

a main digital-analog converter which generates a first tracking voltage for a high speed tracking, where the first tracking voltage corresponds to predetermined upper bits of the digital value; and

a sub digital-analog converter which generates a second tracking voltage for correcting the first tracking voltage to be equal to the reference voltage, where the second tracking voltage corresponds to all the bits, except the predetermined upper bits, of the digital value.

16. (Original) The analog PLL as recited in claim 15, wherein the digital-analog converting means is provided with a binary-thermometer converter which converts the predetermined upper bits to a thermometer code, and outputs the converted thermometer code to the main digital-analog converter, where the main digital-analog converter is segment typed.

17. (Currently Amended) The analog PLL as recited in claim ~~14~~ 12, a unit gain buffer is included for buffering an outputted signal from the main digital-analog converter and the sub digital-analog converter, and for outputting the buffered signal as the tracking voltage.

18. (Original) The analog PLL as recited in claim 17, a switch is included for transferring the tracking voltage outputted from the unit gain buffer to the loop filter.

19. (Original) The analog PLL as recited in claim 13, wherein the reference voltage is determined by charges pumped by the charge pump when the analog PLL is locked.

20. (Original) The analog PLL as recited in claim 17, wherein all the blocks except the register, the digital-analog converting means and the unit gain buffer become disabled during the standby mode.